Remarks

Claims 1-42 were presented in the previous amendment. The Examiner has rejected claims 1-42. By this amendment, claims 7-8, 17, 21, 25, 29-42 are canceled, and claims 1-6, 9-16, 18-20, 22-24, and 26-28 are amended. Thus, claims 1-6, 9-16, 18-20, 22-24, and 26-28 remain in this application.

The Examiner rejected claims 1-3, 5-6, 8-12, 15-17, 19-20, 22-26, 29-31, 33-34, and 36-40 under 35 USC §102(b) as being anticipated by Nemirovsky (DISC, A Dynamic Stream Computer). More specifically, the examiner stated that Nemirovsky taught the invention as claimed including a processor executing a plurality of streams, a set of function resources page, interrupt logic and interrupts directed to one or more specific streams. Applicant respectfully suggests that his reading of Nemirovsky is a bit different. Applicant agrees with the examiner in that Nemirovsky discloses a processor executing a plurality of streams, and interrupt logic. However, Applicant does not believe that the interrupt logic is directed at one *or more* specific streams. Rather, Nemirovsky states that "Every IS (instruction stream) has *one* interrupt register (IR) and *one* mask register (MR). On DISC1 the interrupt registers contain 8 bits, bit 7 is the highest priority, bit 0 is the lowest priority (or background or normal mode of running). Interrupt 7 to 1 are vectored interrupts.... [sic] When no bit of the IS is set, the instruction stream will not be scheduled (not active). Once an interrupt is requested, if it is the highest priority one pending, a vector interrupt will be generated. The next instruction that belongs to ***that*** IS will be started at the address given by the vector interrupt." at page 167 of Applicant's copy of Nemirovsky, [emphasis added]. Applicant understands this to mean that Nemirovsky teaches the use of an interrupt register for each instruction stream, which defines the priority of interrupts for that instruction stream. Applicant has reviewed Nemirovsky and has not found any teaching of the use of interrupt mapping logic to allow mapping of an interrupt to one or more instruction streams.

With respect to claim 1, it is repeated below for ease of reference:

Claim 1 (currently amended): A multi-streaming processor comprising:

a plurality of hardware streams for streaming one or more instruction threads;

a set of functional resources coupled to said hardware streams for processing instructions from said streams;

interrupt detection logic, coupled to interrupt signals, for providing said interrupt signals to the processor;

interrupt mapping logic, for providing configurable interrupt mapping of said interrupt signals to ones of said plurality of streams; and

interrupt logic, coupled to said interrupt mapping logic, for interrupting one or more of said streams according to said configurable interrupt mapping provided by said interrupt mapping logic;

wherein through said interrupt logic, said interrupts are detected, and at the time of their detection said ones of said plurality of streams are directed to process said interrupts.

Claim 1, as amended, particularly recites "interrupt mapping logic, for providing configurable interrupt mapping of said interrupt signals to ones of said plurality of streams". Applicant respectfully suggests that such mapping of interrupt signals to one or more streams is nowhere taught, suggested, or even hinted at by Nemirovsky. Further, nothing in Nemirovsky is directed at utilization of such mapping logic to, upon interrupt detection, to direct one or more streams to process the interrupts. For these reasons, Applicant respectfully suggests that claim 1, as amended, is novel and non-obvious over Nemirovsky. Applicant requests the Examiner to withdraw his rejection of this claim as amended.

Claim 2 as amended is repeated below for ease of reference:

Claim 2 (currently amended) The processor of claim 1 wherein one of said plurality of interrupts may be mapped to two or more of said plurality of hardware streams.

The examiner indicated that Nemirovsky taught one exception or interrupt directed to two or more streams (page 63) and two or more interrupts or exceptions are directed to one stream (page 63). Applicant is confused. Applicant's copy of Nemirovsky extends from page 163 to page 171. Applicant therefore does not know what page 63 is, as referred to by the Examiner. However, nowhere can applicant find a teaching in Nemirovsky which

maps an interrupt to more than one instruction stream. In fact, applicant has converted a .pdf of Nemirovsky into an electronically searchable format, and searched for every instance of the term interrupt. The result of this search confirms Applicant's statement that nowhere does Nemirovsky teach the mapping of an interrupt to more than one interrupt. In fact, Nemirovsky teaches just the opposite. In Applicant's copy, page 164, 2d column, lines 13-17, Nemirovsky states "It is thus possible to assign an interrupt to *a given stream* which begins processing effectively in parallel and at *a given level* of partitioned throughput ... (emphasis added). Nemirovsky continues to show an advantage of actually not allowing that interrupt to impact the throughput of the other instruction streams by that interrupt! Further, on page 169, column 1, lines 45-48 Nemirovsky states "By *dedicating a stream to a particular interrupt*, we can achieve very high figures of merit... (emphasis added)" Thus, from Applicant's reading of Nemirovsky, every use of the term interrupt implies that an interrupt is dedicated to a particular instruction stream, not mapped to one or more instruction streams. For these reasons, Applicant respectfully requests the Examiner to remove his rejection of this claim. Alternatively, Applicant requests that the Examiner provide him with an exact copy of the reference used by the examiner (so applicant can harmonize the examiner's page reference to the art), indicating page and line number where examiner believes mapping of an interrupt to more than one instruction stream is taught.

With respect to claims 3-6 and 9-14 as amended, these depend either directly or indirectly from claim 1 and add further limitations that are neither anticipated nor obviated by Nemirovsky. For all of the reasons stated above with respect to claims 1 and 2, applicant respectfully requests the examiner to withdraw his rejection of these claims.

Claims 7-8 have been canceled.

With respect to claim 15, it is repeated below as amended for ease of reference:

15. A method for processing an interrupt in a multi-stream processor having a plurality of hardware streams, comprising:

detecting the interrupt and passing the detected interrupt to interrupt mapping logic;

determining, using the interrupt mapping logic, which ones of the plurality of hardware streams are to be interrupted by the interrupt; and

interrupting the ones of the plurality of hardware streams that are to be interrupted by the interrupt.

Claim 15 specifically recites a method for processing an interrupt in a multi stream processor where interrupt mapping logic determines which ones of a plurality of hardware streams are to be interrupted by the interrupt. As mentioned above with respect to claims 1 and 2, applicant cannot find any teaching in Nemirovsky where an interrupt is mapped to more than one instruction stream. For this reason, and for those stated above with respect to claim 1, applicant respectfully requests the examiner to withdraw his rejection of this claim.

With respect to claims 16, 18-20, 22-24, 26-28, these depend either directly or indirectly from claim 15 and add further limitations that are neither anticipated nor obviated by Nemirovsky. For all of the reasons stated above with respect to claims 1, 2 and 15, applicant respectfully requests the examiner to withdraw his rejection of these claims.

Applicant has reviewed the file history of office actions and amendments to date and wishes to respond to one further note by the examiner. More specifically, the examiner stated that "applicant's admission on paper no. 8, last paragraph of page 8 continued on to page 9, set forth that conditional and dynamic mapping is well-known in the art." Applicant wishes to make clear that mapping of an interrupt to an instruction stream was taught by Nemirovsky. However, what was not taught by Nemirovsky, or admitted in the file history, is the novel feature of the present invention, which is the mapping, whether static or dynamic, of an interrupt to one or more hardware streams within a multi-streaming processor.

For all of the above reasons, applicant respectfully requests the examiner to withdraw his rejection of all of the remaining claims, and that a timely Notice of Allowance be issued in this case.

Applicant earnestly requests the examiner to telephone him at the direct dial number printed below if the examiner has any questions or suggestions concerning the application.

Respectfully submitted,

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"EXPRESS MAIL" mailing label number EO002518067US. Date of Deposit 8-26-04. I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 C.F.R. §1.10 on the date shown above and is addressed to the U.S. Commissioner of Patents and Trademarks, Alexandria, VA, 22313.

By: Vicki J Hoy